Docket No.: BBNT-P01-128
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Milliken et al.

Application No.: 09/938,921

Confirmation No.: 3501

Filed: August 24, 2001

Art Unit: 2141

For: TERNARY CONTENT ADDRESSABLE MEMORY EMBEDDED IN A CENTRAL PROCESSING UNIT

Examiner: Q. N. Nguyen

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in response to the non-final Office Action, dated October 5, 2006, which re-opened prosecution of the present application, and in support of the Notice of Appeal, filed January 2, 2007. A Petition for One Month Extension of Time is being filed with this Appeal Brief.

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is: BBN Technologies Corp.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-16 and 18-21 are pending in this application. Claim 17 was previously canceled without prejudice or disclaimer.

Claims 1-16 and 18-21 were rejected in the Office Action, dated October 5, 2006, and are the subject of the present appeal. These claims are reproduced in the Claim Appendix of this Appeal Brief.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Office Action, dated October 5, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In the paragraphs that follow, a concise explanation of the independent claims and the claims reciting means-plus-function or step-plus-function language that are involved in this appeal will be provided by referring, in parenthesis, to examples of where support can be found in the specification and drawings.

Claim 1 recites a central processing unit (CPU) (100, Fig. 1) in a network device. The central processing unit includes an arithmetic logic unit (140, Fig. 1); and a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations (260, Fig. 2; Fig. 5; pg. 10, para. 0030; pg. 15, para. 0042).

Claim 16 recites a method for processing packets in a network device. The method includes receiving a packet (pg. 5, para. 0018; pg. 12, para. 0035; pg. 15, para. 0043); and processing the packet using a ternary content addressable memory resident within an arithmetic logic unit of the network device (pg. 15, paras. 0042 and 0043).

Claim 20 recites a system for forwarding packets in a network device. The system includes means for receiving at least one packet (130, Fig. 1; pg. 5, para. 18; pg. 6, para. 0021; pg. 12, para. 0035; pg. 15, para. 0043); and means for processing the packet using a ternary content addressable

memory (260, Fig. 2) resident within a central processing unit (100, Fig. 1) of the network device (260, Fig. 2; 100, Fig. 1; 130, Fig. 1; pg. 6, para. 0021; pg. 15, paras. 0042 and 0043).

Claim 21 recites an arithmetic logic unit (140) comprising a register unit (250, Fig. 2); an operations unit (270, Fig. 2); and a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit (260, Fig. 2; pg. 9, para. 0028; pg. 10, para. 0030; pg. 11, para. 0034).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claim 21 stands rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter.

B. Claims 1-6, 8-15, and 20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Curtis et al. (U.S. Patent No. 6,000,016) in view of Nataraj et al. (U.S. Patent No. 6,757,779).

C. Claims 7, 16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Curtis et al. in view of Nataraj et al., and further in view of Zuraski, Jr. et al. (U.S. Patent No. 6,560,740).

D. Claim 21 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Zuraski, Jr. et al. in view of Nataraj et al.

VII. ARGUMENT

A. The rejection of claim 21 under 35 U.S.C. § 101 as allegedly directed to non-statutory subject matter should be reversed.

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

1. Claim 21.

35 U.S.C. § 101 provides:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Thus, 35 U.S.C. § 101 defines four categories of inventions that are deemed to be appropriate subject matter of a patent: processes, machines, manufactures, and compositions of matter.

Claim 21 is directed to an arithmetic logic unit that includes a register unit; an operations unit; and a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit. Clearly, claim 21 falls under the category of a "machine," which is one of the four enumerated categories of patentable subject matter recited in 35 U.S.C. § 101. Thus, claim 21 is directed to patentable subject matter.

In the Office Action, the Examiner alleges:

> Claim 21 does not appear to result in a physical transformation nor does it appear to produce a useful, concrete, and tangible result. Specially, it does not appear to produce a tangible result because merely describing "a ternary content addressable memory coupled to a register unit and an operations unit within an arithmetic logic unit" fails to describe, to use, or to make available to use, the result of the description in order to enable its functionality and usefulness to be realized. The practical application is not explicitly recited in the claim nor does it flow inherently therefrom, thus, claim 21 appears to be directed to non-statutory subject matter

(emphasis in the original) (Office Action, pg. 3). Appellant disagrees.

At the outset, Appellant notes that the Examiner does not address whether claim 21 falls under one of the four enumerated categories of patentable subject matter recited in 35 U.S.C. § 101. Accordingly, the Examiner does not establish a *prima facie* basis for denying patentability under 35 U.S.C. § 101.

Contrary to the Examiner's allegations, 35 U.S.C. § 101 does not require that a claim that falls under one of the four enumerated categories of patentable subject matter recited in 35 U.S.C. § 101 include a physical transformation or that such a claim produce a useful, concrete, and tangible result.

For at least the foregoing reasons, Appellant submits that the rejection of claim 1 under 35 U.S.C. § 101 is improper. Accordingly, Appellant respectfully requests that the rejection be reversed.

B. The rejection of claims 1-6, 8-15, and 20 under 35 U.S.C. § 103(a) as unpatentable over Curtis et al. in view of Nataraj et al. should be reversed.

In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985).

Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

1. Claims 1-4 and 11-15.

Claim 1 is directed to a central processing unit (CPU) in a network device. The CPU includes an arithmetic logic unit and a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations. Curtis et al. and Nataraj et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, Curtis et al. and Nataraj et al. do not disclose or suggest a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations. The Examiner relies on Curtis et al. for allegedly disclosing a content addressable memory that is operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations (Office Action, pg. 4). The Examiner correctly acknowledges, however, that Curtis et al. does not disclose a ternary content addressable memory (Office Action, pg. 5). Thus, Curtis et al. cannot disclose a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations, as recited in claim 1.

The Examiner relies on element 304/404 of Nataraj et al. as allegedly corresponding to a ternary content addressable memory (Office Action, pg. 5). Appellant submits that, regardless of the accuracy of the Examiner's allegation, Nataraj et al. does not disclose or suggest that element 304/404 is operatively coupled to an arithmetic logic unit within a CPU and configured to perform

one or more matching operations, as would be required by claim 1 based on the Examiner's interpretation of Nataraj et al. In fact, Nataraj et al. does not even disclose an arithmetic logic unit.

With respect to motivation, the Examiner alleges:

> it would have been obvious ... to incorporate the feature of the content addressable memory (CAM) is a ternary content addressable memory (TCAM), as disclosed by Nataraj, into the teaching of Curtis, since a ternary CAM requires a smaller number of table entries to represent each hierarchical address than a binary CAM (a single ternary entry "1XX" can be represented be represented by 4 binary entries "100", "101", "110" and "111"), therefore, using a ternary CAM in place of a binary CAM would reduce a number of searches of the CAM needed in the worst case to find a matching entry

(Office Action, pg. 5). Appellant submits that the Examiner's motivation is merely a conclusory statement regarding an allegedly benefit of incorporating a ternary content addressable memory into Curtis et al. Such motivation statements are insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995), where it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. The Examiner does not point to any section of Curtis et al., Nataraj et al., or knowledge generally available to one skilled in the art at the time of Appellant's invention to provide the alleged motivation.

Appellant notes that, contrary to the Examiner's allegation, one skilled in the art at the time of Appellant's invention would recognize that a content addressable memory and a ternary content addressable memory are not simply interchangeable pieces of logic, allowing one to simply upgrade a content addressable memory with a ternary content addressable memory. The Examiner does not point to any section of Curtis et al., Nataraj et al., or knowledge generally available to one skilled in the art at the time of Appellant's invention to explain why one skilled in the art at the time of

Appellant's invention would have been motivated to change the operation of the Curtis et al. system to include a ternary content addressable memory. Appellant submits that the Examiner's purported motivation to combine the cited references is merely conclusory and based on impermissible hindsight.

For at least the foregoing reasons, Appellant submits that the rejection of claim 1 under 35 U.S.C. § 103(a) based on Curtis et al. and Nataraj et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

Since claims 2-4 and 11-15 depend from claim 1, Appellant requests that the rejection of these claims be reversed for at least the reasons given above with respect to claim 1.

2. Claim 5.

Claim 5 depends from claim 1. Therefore, claim 5 is patentable over Curtis et al. and Nataraj et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Curtis et al. and Nataraj et al.

Claim 5 recites that the one or more matching operations include a packet stuff/unstuff operation. The Examiner relies on the Abstract, col. 2, lines 39-44, and col. 6, lines 1-31, of Curtis et al. and col. 14, lines 27 to col. 15, line 13, of Nataraj et al. for allegedly disclosing the above feature of claim 5 (Office Action, pg. 6). Appellant respectfully disagrees with the Examiner's interpretation of Curtis et al. and Nataraj et al.

At the outset, Appellant notes that the Examiner admits that Curtis et al. does not disclose a ternary content addressable memory (Office Action, pg. 5). Therefore, Appellant submits that it is unreasonable for the Examiner to rely on Curtis et al. for allegedly disclosing a ternary content

addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet stuff/unstuff operation, as recited in claim 5.

Nevertheless, in the Abstract, Curtis et al. discloses:

> A microprocessor includes a register file that contains registers for storing pieces of data for use by execution units that receive the pieces of data through source ports. A bypass cache includes data registers into which pieces of data from the execution units are written. Data can be written to and read from the bypass cache in fewer clocks cycles than it can be written to and read from the register file. A content addressable memory array (CAM) includes address registers into which destination addresses are written which correspond to the pieces of data in the data registers. In the case of a particular piece of data, the particular data register into which the piece of data is written and the particular address register into which the corresponding destination address is written is controlled by the position of a write pointer provided by a rotating write pointer unit. The CAM includes a comparators that compare the destination address with a source address. If there is a match, a read port is enabled which provides the piece of data in the corresponding data register to conductors leading to the source port. Multiplexers select between pieces of data in the register file and a pieces of data in the data registers of the bypass cache.

This section of Curtis et al. discloses a content addressable memory array that includes address registers into which destination addresses are written. This section of Curtis et al. does not disclose or suggest a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet stuff/unstuff operation, as recited in claim 5.

At col. 2, lines 39-44, Curtis et al. discloses:

> The CAM receives destination addresses of the pieces of data and source addresses of desired pieces of data, and when there is a match between one of the source addresses and one of the destination addresses, the CAM provides a signal to activate a corresponding one of the read ports.

This section of Curtis et al. discloses a content addressable memory that provides a signal to activate a corresponding one of the read ports when there is a match between one of the source addresses

and one of the destination addresses. This section of Curtis et al. does not disclose or suggest a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet stuff/unstuff operation, as recited in claim 5.

At col. 6, lines 1-31, Curtis et al. discloses:

> Comparators 160, 162, 164, and 166 also receive the destination addresses in address registers A1, A2, A3, and A4, respectively. As illustrated in FIG. 5, comparator 160 receives the six source addresses on conductors 124-1, 124-2, 124-3, 124-4, 124-5, and 124-6. Comparator 162 also receives the same six source addresses on conductors 124-1, 124-2, 124-3, 124-4, 124-5, and 124-6. (Comparator 160 may be considered six comparators.) Destination addresses are provided to comparators 160 and 162 from registers A1 and A2 through conductors 168 and 176, respectively. If a source address on one of conductors 124 matches the destination address in address register A1, a signal (which may be called a pointer) is asserted at a corresponding one of outputs 210-1, 210-2, 210-3, 210-4, 210-5, and 210-6 which form outputs 210 of comparator 160. Outputs 210-1, 210-2, 210-3, 210-4, 210-5, and 210-6 are connected to conductors 150-1, 150-2, 150-3, 150-4, 150-5, or 150-6, respectively, which form conductors 150. For example, if the source address on conductors 124-1 is 011110, it matches the contents of address register A1 (see FIG. 4), and a signal from output 210-1 is asserted on conductor 150-1. Likewise, if the source address on conductors 124-3 is 011110, it also matches the contents of address register A1, and a signal from output 210-3 is asserted on conductor 150-3. The other comparators are the same as comparator 160. For example, comparator 162 includes outputs 212. If conductors 124-5 includes source address 110000, then a signal from output 212-5 will be asserted on conductor 152-5 because address register A2 contains 110000. Signals on individual ones of conductors 154 and 156 are asserted if there is a match in comparators 164 or 166.

This section of Curtis et al. discloses matching source addresses and destination addresses. This section of Curtis et al. does not disclose or suggest a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet stuff/unstuff operation, as recited in claim 5.

At col. 14, line 27 to col. 15, lines 13, Nataraj et al. discloses inserting and deleting policy statements into a CAM array 404. This section of Nataraj et al. does not disclose or suggest a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet stuff/unstuff operation, as recited in claim 5.

For at least the foregoing reasons, Appellant submits that the rejection of claim 5 under 35 U.S.C. § 103(a) based on Curtis et al. and Nataraj et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

3. Claim 6.

Claim 6 depends from claim 1. Therefore, claim 6 is patentable over Curtis et al. and Nataraj et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Curtis et al. and Nataraj et al.

Claim 6 recites that the one or more matching operations include a packet classification operation. The Examiner relies on the Abstract, col. 2, lines 39-44, and col. 6, lines 1-31, of Curtis et al. and col. 9, lines 33-63, of Nataraj et al. for allegedly disclosing the above feature of claim 6 (Office Action, pg. 6). Appellant respectfully disagrees with the Examiner's interpretation of Curtis et al. and Nataraj et al.

At the outset, Appellant notes that the Examiner admits that Curtis et al. does not disclose a ternary content addressable memory (Office Action, pg. 5). Therefore, Appellant submits that it is unreasonable for the Examiner to rely on Curtis et al. for allegedly disclosing a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to

perform one or more matching operations, where the one or more matching operations include a packet classification operation, as recited in claim 6.

Nevertheless, in the Abstract, Curtis et al. discloses:

> A microprocessor includes a register file that contains registers for storing pieces of data for use by execution units that receive the pieces of data through source ports. A bypass cache includes data registers into which pieces of data from the execution units are written. Data can be written to and read from the bypass cache in fewer clocks cycles than it can be written to and read from the register file. A content addressable memory array (CAM) includes address registers into which destination addresses are written which correspond to the pieces of data in the data registers. In the case of a particular piece of data, the particular data register into which the piece of data is written and the particular address register into which the corresponding destination address is written is controlled by the position of a write pointer provided by a rotating write pointer unit. The CAM includes a comparators that compare the destination address with a source address. If there is a match, a read port is enabled which provides the piece of data in the corresponding data register to conductors leading to the source port. Multiplexers select between pieces of data in the register file and a pieces of data in the data registers of the bypass cache.

This section of Curtis et al. discloses a content addressable memory array that includes address registers into which destination addresses are written. This section of Curtis et al. does not disclose or suggest a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet classification operation, as recited in claim 6.

At col. 2, lines 39-44, Curtis et al. discloses:

> The CAM receives destination addresses of the pieces of data and source addresses of desired pieces of data, and when there is a match between one of the source addresses and one of the destination addresses, the CAM provides a signal to activate a corresponding one of the read ports.

This section of Curtis et al. discloses a content addressable memory that provides a signal to activate a corresponding one of the read ports when there is a match between one of the source addresses and one of the destination addresses. This section of Curtis et al. does not disclose or suggest a

ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet classification operation, as recited in claim 6.

At col. 6, lines 1-31, Curtis et al. discloses:

> Comparators 160, 162, 164, and 166 also receive the destination addresses in address registers A1, A2, A3, and A4, respectively. As illustrated in FIG. 5, comparator 160 receives the six source addresses on conductors 124-1, 124-2, 124-3, 124-4, 124-5, and 124-6. Comparator 162 also receives the same six source addresses on conductors 124-1, 124-2, 124-3, 124-4, 124-5, and 124-6. (Comparator 160 may be considered six comparators.) Destination addresses are provided to comparators 160 and 162 from registers A1 and A2 through conductors 168 and 176, respectively. If a source address on one of conductors 124 matches the destination address in address register A1, a signal (which may be called a pointer) is asserted at a corresponding one of outputs 210-1, 210-2, 210-3, 210-4, 210-5, and 210-6 which form outputs 210 of comparator 160. Outputs 210-1, 210-2, 210-3, 210-4, 210-5, and 210-6 are connected to conductors 150-1, 150-2, 150-3, 150-4, 150-5, or 150-6, respectively, which form conductors 150. For example, if the source address on conductors 124-1 is 011110, it matches the contents of address register A1 (see FIG. 4), and a signal from output 210-1 is asserted on conductor 150-1. Likewise, if the source address on conductors 124-3 is 011110, it also matches the contents of address register A1, and a signal from output 210-3 is asserted on conductor 150-3. The other comparators are the same as comparator 160. For example, comparator 162 includes outputs 212. If conductors 124-5 includes source address 110000, then a signal from output 212-5 will be asserted on conductor 152-5 because address register A2 contains 110000. Signals on individual ones of conductors 154 and 156 are asserted if there is a match in comparators 164 or 166.

This section of Curtis et al. discloses matching source addresses and destination addresses. This section of Curtis et al. does not disclose or suggest a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet classification operation, as recited in claim 6.

At col. 9, lines 33-63, Nataraj et al. discloses:

> FIG. 5 summarizes the classification or filtering function 500 (i.e., search or compare operation) performed by CAM device 402 for an incoming packet according to a policy stored in ternary CAM 404. An incoming packet received by a policy-based router incorporating system 400 is initially processed to determine the policy field information. The policy field information is provided to system 400 as policy search key 409. At step 502, the policy fields of policy search key 409 are compared with the policy statements stored in ternary CAM array 404. For each policy statement that matches the policy search key, the corresponding match line ML_0 -ML_{N-1} is asserted. If no match is found, then the process stops at step 504.
>
> At step 506, priority logic 410 determines PNUM and identifies its location in priority memory 408. The identified location is provided on internal address lines IAD_0 -IAD_{N-1} to encoder 412. At step 508, encoder 412 determines the address of the identified location in priority index table 406. This encoded address is also the logical address of the highest priority matching policy statement in ternary CAM array 404. Encoder 412 outputs the encoded address to HPM bus 416. The encoded address can then be used at step 510 to access the corresponding route information in memory 414. Steps 508 and/or 510 may be omitted when encoder 412 is removed from CAM device 402, and priority logic 410 may directly access the route information in memory 414.
>
> For another embodiment, IAD_0 -IAD_{N-1} are provided to CAM array 404 to access the highest priority matching policy statement, which may then be read from CAM device 402. Alternatively, HPM bus 416 may be provided to CAM array 404 (e.g., through a decoder) to access the highest priority matching policy statement.

This section of Nataraj et al. discloses a classification or filtering function 500 that is performed by CAM device 402 for an incoming packet according to a policy stored in ternary CAM 404. This section of Nataraj et al. does not disclose or suggest a ternary content addressable memory that is operatively coupled to an arithmetic logic unit within a CPU. Thus, this section of Nataraj et al. cannot disclose or suggest a ternary content addressable memory operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet classification operation, as recited in claim 6.

Even assuming, for the sake of argument, that the above section of Nataraj et al. could reasonably be construed as disclosing a ternary content addressable memory that is operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet classification operation (a point that Appellant does not concede), Appellant submits that one skilled in the art at the time of Appellant's invention would not have been motivated to incorporate this alleged teaching of Nataraj et al. into the Curtis et al. system, absent impermissible hindsight. The Examiner does not provide any motivation as to why one would seek to incorporate Nataraj et al.'s alleged disclosure of a ternary content addressable memory that is operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, where the one or more matching operations include a packet classification operation into the Curtis et al. system. Thus, a *prima facie* case of obviousness has not been established with respect to claim 6.

For at least the foregoing reasons, Appellants submit that the rejection of claim 6 under 35 U.S.C. § 103(a) based on Curtis et al. and Nataraj et al. is improper. Accordingly, Appellants request that the rejection be reversed.

4. Claims 8-10.

Claim 8 depends from claim 1. Therefore, claim 8 is patentable over Curtis et al. and Nataraj et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Curtis et al. and Nataraj et al.

Claim 8 recites that the CPU includes a first register configured to store a first 32-bit operand and a second register configured to store a second 32-bit operand. The Examiner admits

that Curtis et al. does not disclose the recited first and second registers (Office Action, pg. 6). The Examiner relies on elements C1 and C2 in Nataraj et al.'s Fig. 21 as allegedly corresponding to the recited first and second registers and points to col. 37, line 46 to col. 38, line 24, of Nataraj et al. for support (Office Action, pp. 6-7). Appellant respectfully disagrees with the Examiner's interpretation of Nataraj et al.

Elements C1 and C2 in Nataraj et al.'s Fig. 21 correspond to comparand register segments (col. 37, lines 50-52). With this interpretation in mind, Nataraj et al. does not disclose or suggest that a CPU includes comparand register segments C1 and C2, as would be required by claim 8 based on the Examiner's interpretation of Nataraj et al.

At col. 37, line 46 to col. 38, line 24, Nataraj et al. discloses:

> FIG. 21 illustrates an embodiment of a comparand load circuit which may be used in the exemplary CAM device described above in reference to FIGS. 16-19 (i.e., 64-bit wide data bus 1604, and a CAM array 1601 that includes Z=8 row segments (S1-S8) per row, each row segment having W=32 CAM cells). A comparand register 2103 includes eight comparand register segments, C1-C8, to store as many as eight corresponding comparand segments. Comparand register segments C1, C3, C5 and C7 are coupled to receive comparand data from the lower 32 signal lines of the data bus 1604 (i.e., signal path 2106), while comparand register segments C2, C4, C6 and C8 are coupled to receive comparand data from a multiplexer circuit 2105 via signal path 2108. When the CAM array 1601 is in a x32 configuration, the multiplexer circuit 2105 selects the lower 32 signal lines of the data bus to provide comparand data to comparand register segments C2, C4, C6 and C8, such that all eight comparand register segments are coupled to receive the same 32-bit value from the data bus 1604. When the CAM array 1601 is configured for x64, x128 or x256 operation, the multiplexer circuit 2105 selects the upper 32 signal lines of the data bus to provide comparand data to comparand register segments C2, C4, C6 and C8, such that comparand register segment pairs C1|C2, C3|C4, C5|C6 and C7|C8 are coupled to receive a 64-bit data value from the data bus 1604. In the embodiment of FIG. 21, the multiplexer circuit is controlled by the configuration signal, SZ32 (a component of the CFG signal) to select either the lower or upper half of the data bus 1604 to source data for the even numbered comparand register segments.
>
> Comparand enable signals, CEN[8:1], are generated in accordance with the configuration signals (i.e., SZ32, SZ64, SZ128 and SZ256) and comparand segment

> select signals CSSEL1 and CSSEL0 to enable selected comparand register segments to be loaded with comparand data. More specifically, the configuration signals indicate the size of an incoming comparand word (i.e., x32, x64, x128 or x256) and, when the incoming comparand word is larger than the data bus (i.e., a x128 long comparand word or x256 long comparand word), the CSSEL1 and CSSEL0 signals are used to load a 64-bit component of the long comparand word into the appropriate pair of comparand register segments. In one embodiment, when the comparand word is a 64-bit value (i.e., SZ=64), the 64-bit comparand word is loaded into all four comparand register segment pairs simultaneously. Similarly, when the comparand word is a 32-bit value (i.e., SZ=32), the 32-bit comparand word is loaded into all eight comparand register segments simultaneously.

This section of Nataraj et al. discloses that a comparand register 2103 includes eight comparand register segments C1-C8. This section of Nataraj et al. does not disclose or suggest a CPU that includes comparand register segments C1-C8, as would be required by claim 8 based on the Examiner's interpretation of Nataraj et al.

With respect to motivation, the Examiner alleges:

> it would have been obvious ... to incorporate the feature of a first register configured to store a first 32-bit operand and a second register configured to store a second 32-bit operand, as disclosed by Nataraj, into the teaching of Curtis, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array

and points to col. 22, lines 8-45 of Nataraj et al. for support (Office Action, pg. 7). Appellant submits that the Examiner's motivation is merely a conclusory statement regarding an allegedly benefit of combining Nataraj et al. with Curtis et al. Such motivation statements are insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995), where it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. The Examiner merely provides generalizations regarding alleged

benefits of combining Nataraj et al. with Curtis et al. without providing any realistic motivation for incorporating Nataraj et al.'s comparand register segments into Curtis et al.

At col. 22, lines 8-45, Nataraj et al. discloses that CAM array 1501 can be configured into different width and depth configurations. This section of Nataraj et al. does not explain why one skilled in the art would seek to incorporate Nataraj et al.'s comparand register segments into the Curtis et al. system or that by incorporating these comparand register segments into the Curtis et al. system, " the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array," as the Examiner alleges. Appellant submits that the Examiner's motivation for incorporating Nataraj et al.'s comparand register segments into the Curtis et al. system is based on impermissible hindsight.

For at least the foregoing reasons, Appellant submits that the rejection of claim 8 under 35 U.S.C. § 103(a) based on Curtis et al. and Nataraj et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

Since claims 9 and 10 depend from claim 8, Appellant requests that the rejection of claims 9 and 10 be reversed for at least the reasons given above with respect to claim 8.

5. Claim 20.

Claim 20 is directed to a system for forwarding packets in a network device. The system includes means for receiving at least one packet and means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device. Curtis et al. and Nataraj et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, Curtis et al. and Nataraj et al. do not disclose or suggest means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device. The Examiner does not specifically address the features of claim 20. Instead, the Examiner references the rejection of claim 1 (Office Action, pg. 13). Claim 1, however, does not recite means for processing a packet using a ternary content addressable memory resident within a central processing unit of a network device, as recited in claim 20. Instead, claim 1 recites an arithmetic logic unit; and a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations. The Examiner does not address the specific features recited in claim 20. Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 20.

Nonetheless, the Examiner correctly acknowledges with respect to claim 1 that Curtis et al. does not disclose a ternary content addressable memory (Office Action, pg. 5). Thus, Curtis et al. cannot disclose means for processing a packet using a ternary content addressable memory resident within a central processing unit of a network device, as recited in claim 20.

Further with respect to claim 1, the Examiner relies on element 304/404 of Nataraj et al. as allegedly corresponding to a ternary content addressable memory (Office Action, pg. 5). Assuming, for the sake of argument, that Nataraj et al.'s element 304/404 could reasonably be construed as a ternary content addressable memory, Appellant submits that one skilled in the art at the time of Appellant's invention would not have been motivated to incorporate this ternary content addressable memory into the Curtis et al. system, absent impermissible hindsight. With respect to motivation, the Examiner alleges:

> it would have been obvious ... to incorporate the feature of the content addressable memory (CAM) is a ternary content addressable memory (TCAM), as disclosed by

> Nataraj, into the teach of Curtis, since a ternary CAM requires a smaller number of table entries to represent each hierarchical address than a binary CAM (a single ternary entry "1XX" can be represented be represented by 4 binary entries "100", "101", "110" and "111"), therefore, using a ternary CAM in place of a binary CAM would reduce a number of searches of the CAM needed in the worst case to find a matching entry

(Office Action, pg. 5). Appellant submits that the Examiner's motivation is merely a conclusory statement regarding an allegedly benefit of combining Nataraj et al. with Curtis et al. Such motivation statements are insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995), where it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. The Examiner does not point to any section of Curtis et al., Nataraj et al., or knowledge generally available to one skilled in the art at the time of Appellant's invention to provide the alleged motivation.

Appellant notes that, contrary to the Examiner's allegation, one skilled in the art at the time of Appellant's invention would recognize that a content addressable memory and a ternary content addressable memory are not simply interchangeable pieces of logic, allowing one to simply upgrade a content addressable memory with a ternary content addressable memory. The Examiner does not point to any section of Curtis et al., Nataraj et al., or knowledge generally available to one skilled in the art at the time of Appellant's invention to explain why one skilled in the art at the time of Appellant's invention would have been motivated to change the operation of the Curtis et al. system to include a ternary content addressable memory. Appellant submits that the Examiner's purported motivation to combine the cited references is merely conclusory and based on impermissible hindsight.

For at least the foregoing reasons, Appellants submit that the rejection of claim 20 under 35 U.S.C. § 103(a) based on Curtis et al. and Nataraj et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

C. The rejection of claims 7, 16, 18, and 19 under 35 U.S.C. § 103(a) as unpatentable over Curtis et al. in view of Nataraj et al., and further in view of Zuraski, Jr. et al. should be reversed.

1. Claim 7.

Claim 7 depends from claim 1. The disclosure of Zuraski, Jr. et al. does not remedy the deficiencies in the disclosures of Curtis et al. and Nataraj et al. set forth above with respect to claim 1. Therefore, claim 7 is patentable over Curtis et al., Nataraj et al., and Zuraski, Jr. et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Curtis et al., Nataraj et al., and Zuraski, Jr. et al.

Claim 7 recites that the ternary content addressable memory is located within the arithmetic logic unit. The Examiner admits that Curtis et al. and Nataraj et al. do not disclose this feature (Office Action, pg. 14). The Examiner relies on Fig. 8 and col. 9, lies 47-60, of Zuraski, Jr. et al. for allegedly disclosing "a content addressable memory CAM 82 located within a repair logic unit 70" (Office Action, pg. 14). Appellant submits that the Examiner has misinterpreted the language of claim 7.

Appellant's claim 7 does not recite a content addressable memory located within a repair logic unit. Instead, claim 7 specifically recites that the ternary content addressable memory is located within an arithmetic logic unit. The Examiner does not address this feature in the Office

Action. Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 7.

Zuraski, Jr. et al.'s Fig. 8 depicts a repair logic unit 70, which includes a content addressable memory 82. This figure of Zuraski, Jr. et al. does not disclose or suggest an arithmetic logic unit or a ternary content addressable memory. Thus, this figure of Zuraski, Jr. et al. cannot disclose or suggest a ternary content addressable memory that is located within an arithmetic logic unit, as recited in claim 7. Zuraski, Jr. et al. does not disclose or suggest that repair logic unit 70 is an arithmetic logic unit. One skilled in the art would readily appreciate that an "arithmetic logic unit" is a specific kind of device (typically one with two inputs, a function select input, and one output containing the result of the function applied to the two inputs). A common example of an arithmetic logic unit is the TTL 74181 arithmetic logic unit chip and its various descendants. Zuraski, Jr. et al. in no way discloses or suggests that repair logic unit 70 is implemented as an arithmetic logic unit and the Examiner has not pointed to any section of Zuraski, Jr. et al. that supports this allegation.

With respect to motivation, the Examiner alleges:

> it would have been obvious ... to incorporate the feature of locating the (ternary) content addressable memory within the (arithmetic) logic unit, as disclosed by Zuraski, into the teaching of Curtis-Nataraj, because embedding/integrating the ternary content addressable memory within the arithmetic logic unit would provide support hardware-based searching/matching engine functions by quickly examining incoming packets (address information/signals) and forwarding them to other systems in the network for further processing

(Office Action, pg. 14). Appellant submits that the Examiner's motivation is merely a conclusory statement regarding an allegedly benefit of combining Zuraski, Jr. et al. with Curtis et al. and Nataraj et al. Such motivation statements are insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210

(Fed. Cir. 1995), where it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. The Examiner does not point to any section of Zuraski, Jr. et al., Curtis et al., Nataraj et al., or knowledge generally available to one skilled in the art at the time of Appellant's invention to provide the alleged motivation. Appellant submits that the Examiner's purported motivation to combine the cited references is merely conclusory and based on impermissible hindsight.

For at least the foregoing reasons, Appellant submits that the rejection of claim 7 under 35 U.S.C. § 103(a) based on Curtis et al., Nataraj et al., and Zuraski, Jr. et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

2. Claims 16, 18, and 19.

Claim 16 is directed to a method for processing packets in a network device. The method includes receiving a packet; and processing the packet using a ternary content addressable memory resident within an arithmetic logic unit of the network device. Curtis et al., Nataraj et al., and Zuraski, Jr. et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, Curtis et al., Nataraj et al., and Zuraski, Jr. et al. do not disclose or suggest processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a network device. With respect to claim 16, the Examiner alleges:

> [c]laim 16 recites a method that contains substantially the same limitations as recited in claim 1 and 7; therefore, it is rejected under the same rationale

(Office Action, pg. 14). Appellant submits that claims 1 and 7 do not recite, however, processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a

network device, as recited in claim 16. Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 16.

Nonetheless, with respect to claim 7, which recites a ternary content addressable memory that is located within an arithmetic logic unit, the Examiner admits that Curtis et al. and Nataraj et al. do not disclose this feature (Office Action, pg. 14). The Examiner relies on Fig. 8 and col. 9, lies 47-60, of Zuraski, Jr. et al. for allegedly disclosing "a content addressable memory CAM 82 located within a repair logic unit 70" (Office Action, pg. 14). Appellant submits that the Examiner's allegation does not address the above feature of claim 16.

That is, Appellant's claim 16 does not recite a content addressable memory located within a repair logic unit. Instead, claim 16 specifically recites processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a network device. The Examiner does not address this feature in the Office Action. Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 16.

Zuraski, Jr. et al.'s Fig. 8 depicts a repair logic unit 70, which includes a content addressable memory 82. This figure of Zuraski, Jr. et al. does not disclose or suggest an arithmetic logic unit or a ternary content addressable memory. Thus, this figure of Zuraski, Jr. et al. cannot disclose or suggest processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a network device, as recited in claim 16. Zuraski, Jr. et al. does not disclose or suggest that repair logic unit 70 is an arithmetic logic unit. One skilled in the art would readily appreciate that an "arithmetic logic unit" is a specific kind of device (typically one with two inputs, a function select input, and one output containing the result of the function applied to the two inputs). A common example of an arithmetic logic unit is the TTL 74181 arithmetic logic unit chip

and its various descendants. Zuraski, Jr. et al. in no way discloses or suggests that repair logic unit 70 is implemented as an arithmetic logic unit and the Examiner has not pointed to any section of Zuraski, Jr. et al. that supports this allegation.

With respect to motivation, the Examiner alleges:

> it would have been obvious ... to incorporate the feature of locating the (ternary) content addressable memory within the (arithmetic) logic unit, as disclosed by Zuraski, into the teaching of Curtis-Nataraj, because embedding/integrating the ternary content addressable memory within the arithmetic logic unit would provide support hardware-based searching/matching engine functions by quickly examining incoming packets (address information/signals) and forwarding them to other systems in the network for further processing

(Office Action, pg. 14). Appellant submits that the Examiner's motivation is merely a conclusory statement regarding an allegedly benefit of combining Zuraski, Jr. et al. with Curtis et al. and Nataraj et al. Such motivation statements are insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995), where it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. The Examiner does not point to any section of Zuraski, Jr. et al., Curtis et al., Nataraj et al., or knowledge generally available to one skilled in the art at the time of Appellant's invention to provide the alleged motivation. Appellant submits that the Examiner's purported motivation to combine the cited references is merely conclusory and based on impermissible hindsight.

For at least the foregoing reasons, Appellant submits that the rejection of claim 16 under 35 U.S.C. § 103(a) based on Curtis et al., Nataraj et al., and Zuraski, Jr. et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

Since claims 18 and 19 depend from claim 16, Appellant requests that the rejection of claims 18 and 19 be reversed for at least the reasons given above with respect to claim 16.

C. The rejection of claim 21 under 35 U.S.C. § 103(a) as unpatentable over Zuraski, Jr. et al. in view of Nataraj et al. should be reversed.

1. Claim 21.

Claim 21 is directed to an arithmetic logic unit. The arithmetic logic unit includes a register unit; an operations unit; and a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit. Zuraski, Jr. et al. and Nataraj et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, Zuraski, Jr. et al. and Nataraj et al. do not disclose or suggest an arithmetic logic unit. The Examiner relies on Zuraski, Jr. et al.'s built-in self-test (BIST) logic unit 20 as allegedly corresponding to an arithmetic logic unit (Office Action, pg. 15). Appellant respectfully disagrees with the Examiner's interpretation of Zuraski, Jr. et al.

Contrary to the Examiner's allegation, Zuraski, Jr. et al. does not disclose or suggest that BIST logic unit 20 is an arithmetic logic unit, as "arithmetic logic unit" is commonly known in the art. One skilled in the art would readily appreciate that an "arithmetic logic unit" is a specific kind of device (typically one with two inputs, a function select input, and one output containing the result of the function applied to the two inputs). A common example of an arithmetic logic unit is the TTL 74181 arithmetic logic unit chip and its various descendants. One skilled in the art would readily appreciate that Zuraski, Jr. et al.'s BIST logic unit 20 is not an arithmetic logic unit, as recited in claim 21. The Examiner has not pointed to any section of Zuraski, Jr. et al. that discloses

that BIST logic unit 20 is an arithmetic logic unit or explained why one skilled in the art would construe Zuraski, Jr. et al.'s BIST logic unit 20 as an arithmetic logic unit. Appellant notes that Zuraski, Jr. et al. does not even disclose an arithmetic logic unit.

The disclosure of Nataraj et al. does not remedy the above deficiency in the disclosure of Zuraski, Jr. et al.

Since Zuraski, Jr. et al. and Nataraj et al. do not disclose or suggest an arithmetic logic unit, Zuraski, Jr. et al. and Nataraj et al. cannot disclose an arithmetic logic unit that includes a ternary content addressable memory coupled to a register unit and an operations unit within the arithmetic logic unit, as also recited in claim 21.

The Examiner admits that Zuraski, Jr. et al. does not disclose a ternary content addressable memory and relies on Nataraj et al. for allegedly disclosing this feature (Office Action, pg. 15). With respect to motivation, the Examiner alleges:

> it would have been obvious ... to incorporate the feature of the content addressable memory (CAM) is a ternary content addressable memory (TCAM), as disclosed by Nataraj, into the teaching of Zuraski, since a ternary CAM requires a smaller number of table entries to represent each hierarchical address than a binary CAM (a single ternary entry "1XX" can be represented by 4 binary entries "100", "101", "110" and "111"), therefore, using a ternary CAM in place of a binary CAM would reduce a number of searches of the CAM needed in the worst case to find a matching entry

(Office Action, pg. 16). Appellant submits that the Examiner's motivation is merely a conclusory statement regarding an allegedly benefit of combining Nataraj et al. with Zuraski, Jr. et al. Such motivation statements are insufficient for establishing a *prima facie* case of obviousness. In this respect, Appellant relies upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995), where it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. The Examiner does not

point to any section of Zuraski, Jr. et al., Nataraj et al., or knowledge generally available to one skilled in the art at the time of Appellant's invention to provide the alleged motivation. Appellant submits that the Examiner's purported motivation to combine the cited references is merely conclusory and based on impermissible hindsight.

For at least the foregoing reasons, Appellant submits that the rejection of claim 16 under 35 U.S.C. § 103(a) based on Zuraski, Jr. et al. and Nataraj et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

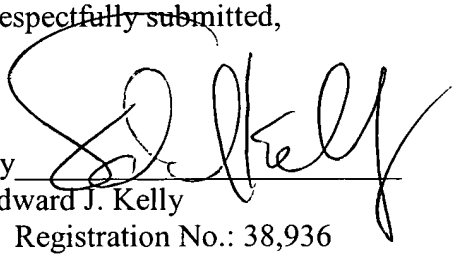
VIII. CONCLUSION

In view of the foregoing arguments, Appellant respectfully solicits the Honorable Board to reverse the Examiner's rejection of claims 1-16 and 18-21 under 35 U.S.C. §§ 101 and 103.

Appellant believes no fee is due with this response other than as reflected on the enclosed Appeal Brief Transmittal. However, if a fee is due, please charge our Deposit Account No. 18-1945, under Order No. BBNT-P01-128 from which the undersigned is authorized to draw.

Dated: April 2, 2007

Respectfully submitted,



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IX. CLAIM APPENDIX

1. In a network device, a central processing unit (CPU) comprising:

an arithmetic logic unit; and

a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations.

2. The CPU of claim 1 wherein the one or more matching operations includes a network packet processing operation.

3. The CPU of claim 2 wherein the packet processing operation includes an address lookup operation.

4. The CPU of claim 3 wherein the address lookup operation includes an Internet Protocol (IP) address lookup operation.

5. The CPU of claim 1 wherein the one or more matching operations includes a packet stuff/unstuff operation.

6. The CPU of claim 1 wherein the one or more matching operations includes a packet classification operation.

7. The CPU of claim 1 wherein the ternary content addressable memory is located within the arithmetic logic unit.

8. The CPU of claim 1 further comprising:

a first register configured to store a first 32-bit operand; and

a second register configured to store a second 32-bit operand.

9. The CPU of claim 8 wherein the ternary content addressable memory performs the one or more matching operations based on at least one of the first or second 32-bit operands.

10. The CPU of claim 8 wherein the ternary content addressable memory includes a memory array including a group of 64-bit entries, and

wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand.

11. The CPU of claim 1 wherein the ternary content addressable memory includes a memory array that includes a group of 64-bit entries.

12. The CPU of claim 11 wherein the memory array comprises 32 entries.

13. The CPU of claim 1 wherein, when performing the one or more matching operations, the ternary content addressable memory is configured to:

compare an operand to a group of entries.

14. The CPU of claim 13 wherein the ternary content addressable memory is further configured to:

set a first flag when the operand fails to match an entry in the group of entries, and

set a second flag when the operand matches multiple entries of the group of entries.

15. The CPU of claim 13 wherein, prior to comparing, the ternary content addressable memory is configured to:

sequentially load the group of entries from a succession of mask/value pairs transferred to the ternary content addressable memory.

16. A method for processing packets in a network device, comprising:

receiving a packet; and

processing the packet using a ternary content addressable memory resident within an arithmetic logic unit of the network device.

18. The method of claim 16 wherein the processing includes performing a matching operation using information in a header of the packet.

19. The method of claim 18 wherein the processing includes a packet classification operation.

20. A system for forwarding packets in a network device, comprising:

means for receiving at least one packet; and

means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device.

21. An arithmetic logic unit comprising:

a register unit;

an operations unit; and

a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.